ABSTRACT OF THE DISCLOSURE

A current mode transfer logic system suitable for driving transmission lines is disclosed. In one embodiment a twisted pair transmission line is terminated in its characteristic line impedance. A signal is formed of two unequal currents, preferably of different polarities as well as magnitudes, that are driven down the two lines. The unequal currents are selectively switched between the two lines creating a logic signal of a differential current drive of unequal current magnitudes. The unequal currents are received and shunted from the distal end of each line via diode connected MOS transistors. The MOS transistors are biased to present a low impedance, but an impedance higher than the terminating resistor. The currents are amplified and converted to useable CMOS voltage levels. In another embodiment the twisted pair is replaced by two parallel transmission lines which are terminated in one resistor, equal to the sum of the characteristic impedances of each line. The terminating resistor is connected between the distal signal carrying conductors of each transmission line. The shields or return paths for each line are tied together at the distal and at the proximate (drive) ends of the line.